Table of Contents: Volume 7 (1994)

Numbers 1/2

Special Issue on Asynchronous Circuit Design for VLSI Signal Processing
Guest Editors: Teresa H. Meng and Sharad Malik

Editorial ..... *Teresa H. Meng and Sharad Malik* 5
Self-Timed Logic Using Current-Sensing Completion Detection (CSCD) ..... *Mark E. Dean, David L. Dill and Mark Horowitz* 7
Performance of Iterative Computation in Self-Timed Rings ..... *Ted E. Williams* 17
High-Level Optimizations in Compiling Process Descriptions to Asynchronous Circuits ..... *Ganesh Gopalakrishnan and Venkatesh Akella* 33
Designing Self-Timed Systems Using Concurrent Programs ..... *Erik Brunvand* 47
Synthesis of Hazard-Free Control Circuits from Asynchronous Finite State Machines Specifications ..... *Tam-Anh Chu* 61
Specification, Synthesis, and Verification of Hazard-Free Asynchronous Circuits ..... *Cho W. Moon, Paul R. Stephan and Robert K. Brayton* 85
A Generalized State Assignment Theory for Transformations on Signal Transition Graphs ..... *Peter Vanbekbergen, Bill Lin, Gert Goossens and Hugo De Man* 101
Specification and Analysis of Self-Timed Circuits ..... *M.A. Kishinevsky, A. Yu. Kondratyev and A.R. Taubin* 117
Linear Programming for Hazard Elimination in Asynchronous Circuits ..... *L. Lavagno, N. Shenoy and A. Sangiovanni-Vincentelli* 137
Verification of Asynchronous Interface Circuits with Bounded Wire Delays ..... *Srinivas Devadas, Kurt Keutzer, Sharad Malik and Albert Wang* 161

Number 3

Special Issue on VLSI Arithmetic
Guest Editors: Vojin G. Oklobdzija and Belle Wei

Introduction ..... *Vojin G. Oklobdzija and Belle Wei* 187
Conventional and On-Line Arithmetic Designs for High-Speed Recursive Digital Filters ..... *John S. Fernando and Miloš D. Ercegovac* 189
ROM Based Methods for Computing the Squaring Operation in Modular Rings ..... *Poornachandra B. Rao and Alexander Skavantzos* 199
An Integrated Multiplier for Complex Numbers ..... *Vojin G. Oklobdzija, David Villeger and Thierry Soulas* 213
Parallel Counter Implementation ..... *Robert F. Jones, Jr. and Earl E. Swartzlander, Jr.* 223
Fast Multiplication in VLSI Using Wave Pipelining Techniques ..... *Fabian Klass, Michael J. Flynn and Ad J. Van de Goor* 233
Fast Multiplier Bit-Product Matrix Reduction Using Bit-Ordering and Parity Generation ..... *Ben C. Drerup and Earl E. Swartzlander, Jr.* 249
Radix-8 Division with Over-Redundant Digit Set ..... *Paolo Montuschi and Luigi Ciminiera* 259
Implementing Division with Field Programmable Gate Arrays ..... *Marianne E. Louie and Miloš D. Ercegovac* 271